[A2-3] Computer-Aided Design of Superconducting SFQ Digital Circuits

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Introduction

- Superconducting SFQ circuits
  - Circuit with 10kJJ @ 20GHz is fabricable now
  - Wiring technology is making progress
- Design conditions/tradeoffs are different from CMOS
  - New design methodology is required
- Computer-aided design is indispensable for system-level design
  - Logic design – synthesis, optimization
  - Layout design – placement, routing

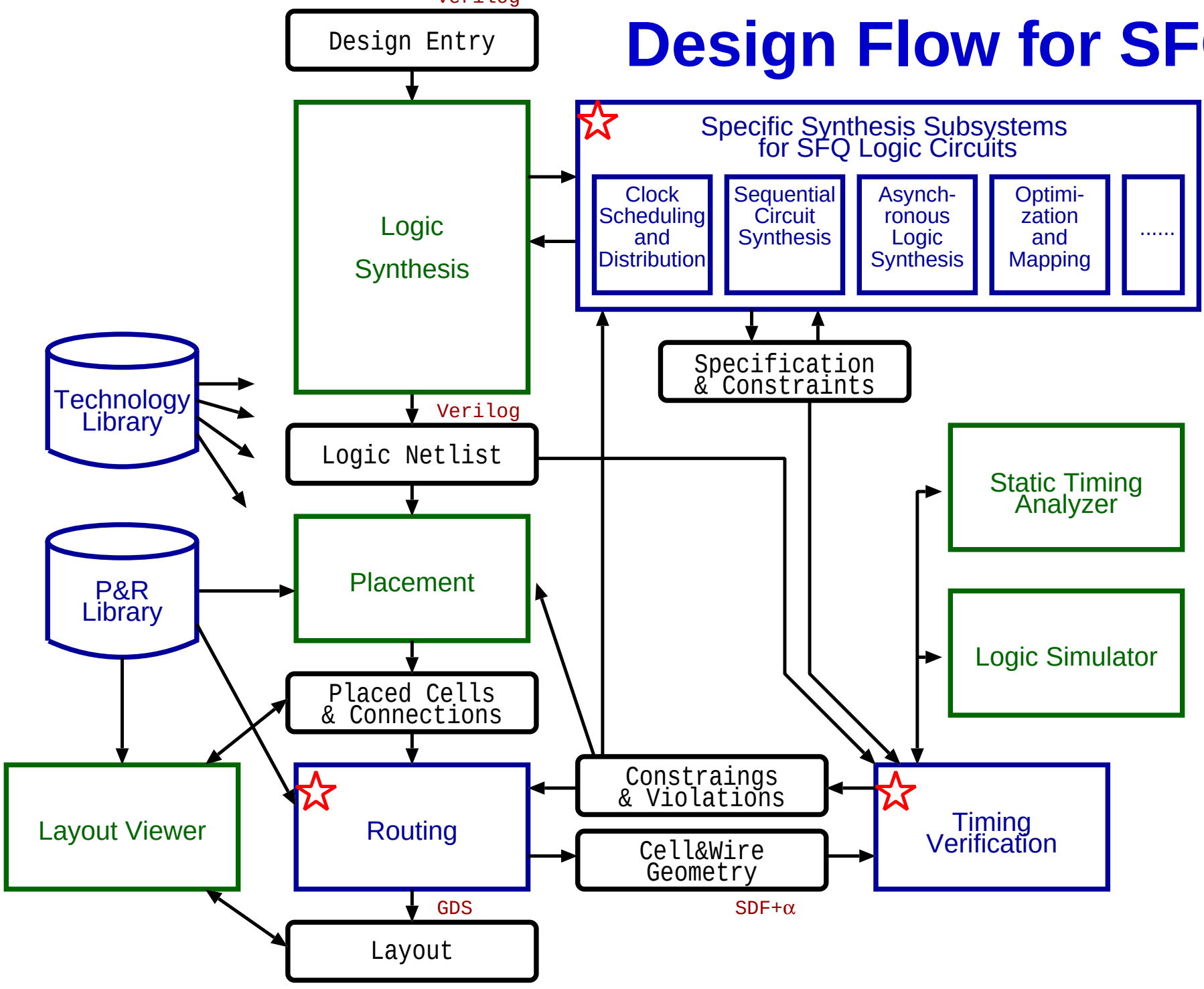
Design of SFQ Digital Circuits

- New ideas for data transmission/processing that make full use of SFQ device
  - Taking into account the properties of SFQ logic cells and wiring
    - Switching speed of JJs vs. signal transmission on wires
    - Logic cell area vs. wiring area
  - Aggressive use of the newly developing transmission lines
- Formalization and solution

Computer-Aided Design for SFQ

- Design flow, algorithms and tools
  - Cell-based design
  - Based on the conventional CMOS design flow
  - Reinforced by dedicated subsystems specific to SFQ
- Cooperation with device/process groups
  - [Inport] Capturing design conditions
  - [Export] Providing algorithms and tools

Design Flow for SFQ



Computer-Aided Design Algorithms

- Logic synthesis and optimization
  - Clock scheduling and distribution
  - Sequential circuit synthesis
  - Asynchronous logic synthesis
  - Circuit optimization
- Placement and routing
  - Placement
  - Routing
  - Timing verification

Logic Synthesis and Optimizatio

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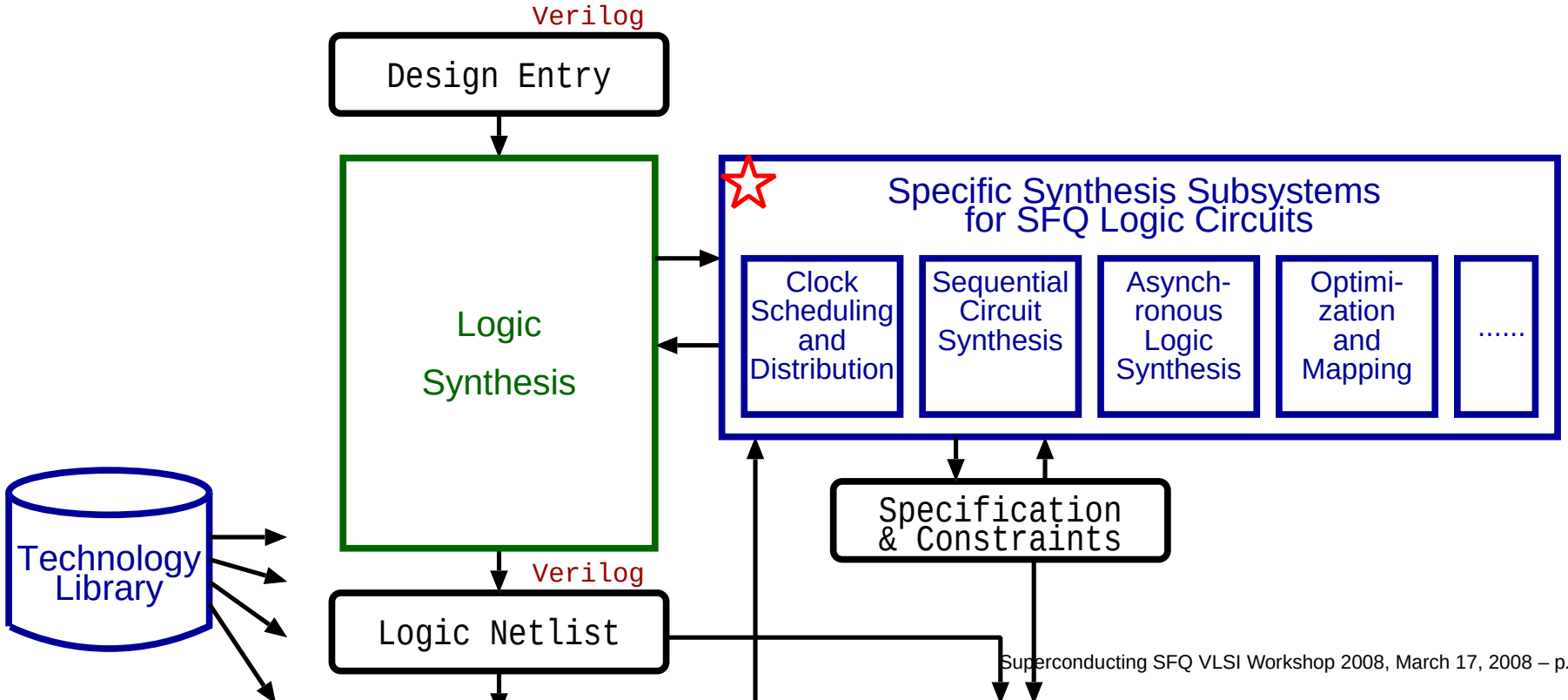
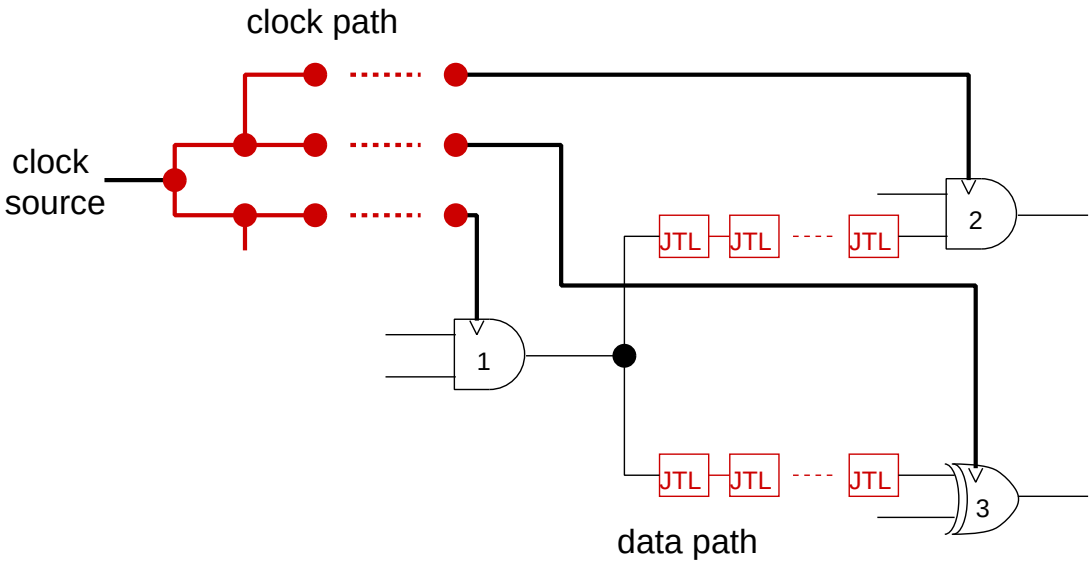


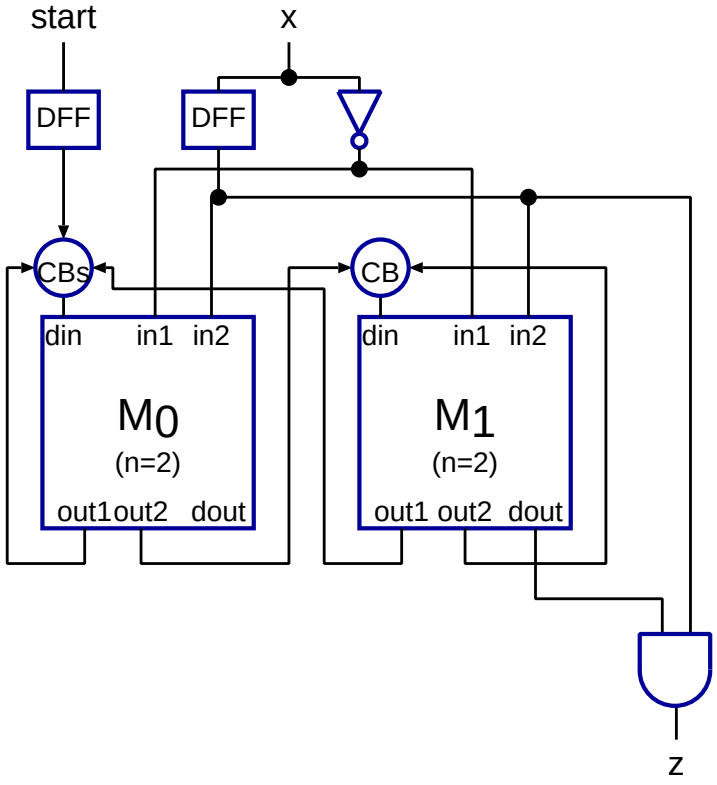
Logic Synthesis and Optimization (1/3)

- Clock scheduling and distribution [2005–]
  - concurrent-flow clocking circuit
  - Pasive-transmission-lines (PTLs) as signal wires
  - Algorithm to determine the signal timing for each logic gate



Logic Synthesis and Optimization (2/3)

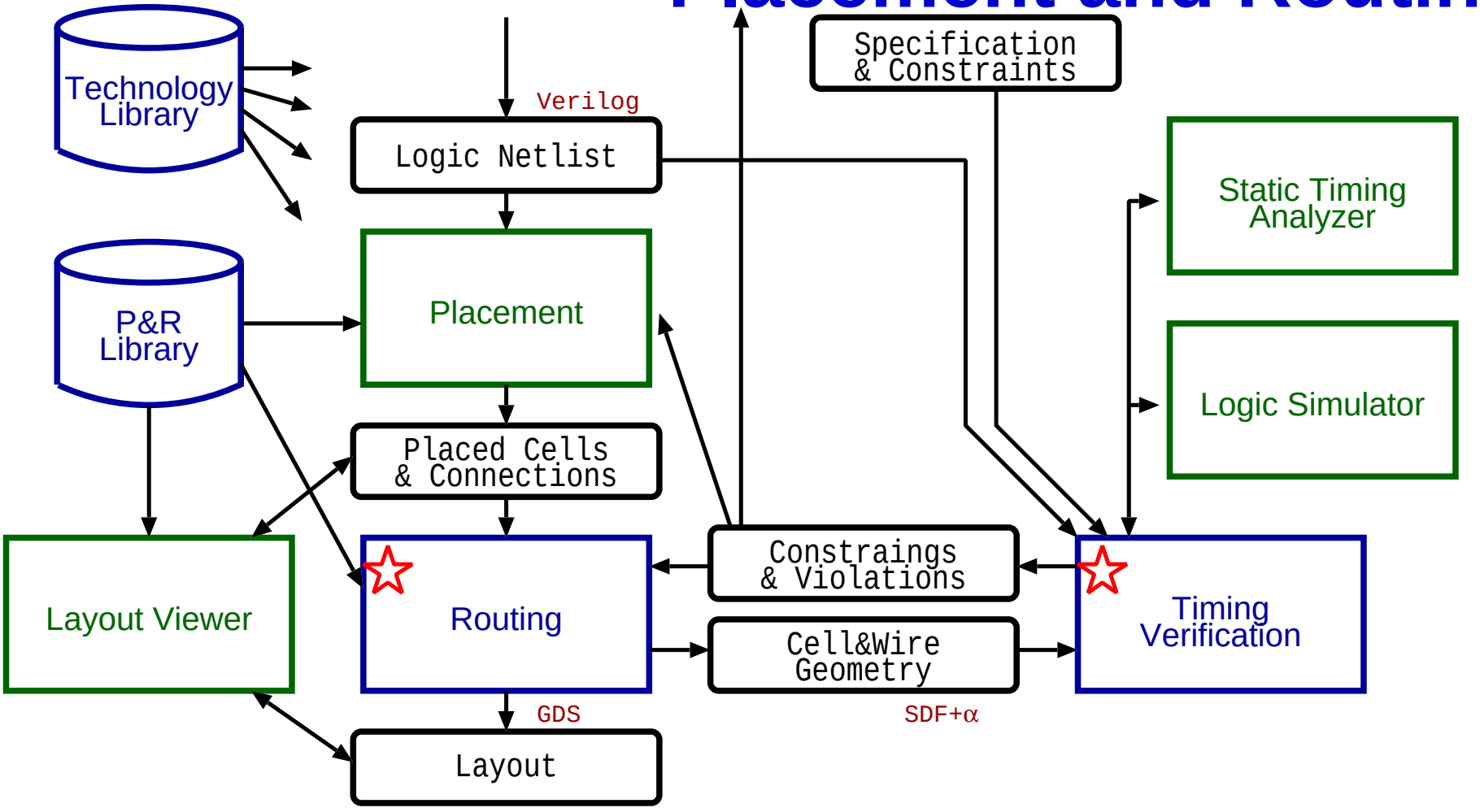
- Sequential circuit synthesis [2007]
  - Synthesis of high-throughput circuit
  - New ‘state module’ is designed
  - One-hot state encoding



Logic Synthesis and Optimization (3/3)

- Asynchronous logic synthesis [2005–2007]
  - Synthesis of delay insensitive dual-rail circuits
  - 2×2-Join as the logic element
  - Newly proposed logic representation RSBDD
- Circuit optimization [2007–]
  - Logic synthesis considering placement and routing
  - Robustness against variation of layout and timing jitters

Placement and Routing



- Placement
- Routing
- Timing verification

Placement and Routing

- Placement
  - Manual procedure using conventional tools
- Routing [2007–]
  - Based on conventional algorithms (e.g. A* algorithm)
  - Considering current SFQ technology
- Timing verification [2007–]
  - Methods to verify behavior of flow-clocking circuits
    - Static timing analysis
    - Signal distribution of flow-clocking
    - Pipeline behavior conforming to the spec

Summary

- Computer-aided design algorithms for SFQ logic design
  - SFQ-specific design issue
  - Formalization and solution
  - Basis of design methods and tools for SFQ
- Design flow for SFQ circuits
  - Making use of CMOS design environment, with SFQ-specific extensions